CLAIMS

1. A process for estimating power consumption, over a given time interval, of digital circuits described at the level of simulated functional elements provided with input/output terminals, characterized in that it comprises the operations of:

emulating, at the hardware level, additional elements associated to said functional elements; said additional emulated elements being able to detect, during emulation of the circuit, at least one signal indicative of the behavior, and hence of power consumption, of the corresponding functional element associated during said time interval; and

acquiring the value of said at least one signal, said value being indicative of the power consumption of said associated functional element in said given time interval.

2. The process according to claim 1, wherein said additional elements are emulated by associating them to an output of the respective functional element.

3. The process according to claim 1, wherein said additional emulated elements are able to detect, during said given time interval:

the number of transitions performed by the corresponding associated functional element; and

the fraction of time in which the state of the corresponding associated functional element is stable,

the value of said number of transitions and said fraction of time being indicative of the power consumption of said functional element during said time interval.

4. The process according to claim 1, wherein it comprises the operation of controlling the acquisition of said at least one signal by means of hardware events monitored by logic analyzers active on the emulator.

5. The process according to claim 1, wherein it comprises the operation of accessing the information stored in said additional emulated elements and the operation of storing said information in view of a subsequent processing.

6. A processing system configured for the implementation of the process according to claim 1.

7. A computer program product directly loadable into the internal memory of a digital computer, comprising software code portions for performing the steps of claim 1 when said product is run on a computer.